REMARKS

I. Status

In the Office Action mailed February 2, 2006, the Examiner noted that claims 1-19 were pending and rejected claims 1-19. Thus, in view of the foregoing, claims 1-19 remain pending for reconsideration, which is requested. No new matter has been added. The applicant respectfully traverses the rejection.

II. Rejection of claims under 35 U.S.C. § 103

Claims 1-2 are rejected under 35 U.S.C. §103(a) as being unpatentable over Harvey et al. (U.S. Patent No. 6,233,668). Page 4 of the Office Action states that claims 8-19 are rejected under the same rational as applied to claims 1-7. Thus, the applicants respectfully traverse the rejections of claims 1-2 and 8-19 under this rejection.

CLAIM 1

Claim 1 recites numerous limitations that are not taught or suggested in Harvey et al. By way of example, Claim 1 recites a method in a system of multiple processors wherein there is a first and second instance of a program, the first instance of the program referring to a virtual memory address (VMA) in a page table to obtain a pointer to a memory location of a memory coupled to a first processor, the second instance of the program referring to a VMA in a page table to obtain a memory location of a memory coupled to a second processor, and wherein **the VMA referred to by each of the first and second instances of the program is the same.** In contrast to the present invention which recites to VMAs for a first and second processor, Harvey et al. discloses a main memory with private page tables for processes A, B, and C (see FIG 1, main memory 14, process elements 24, 26, and 28).

The Examiner admits that Harvey et al. implicitly fails to teach claim 1 and further alleges that it is "obvious that during execution of the instance of the program refers to memory address using page tables and pointers to refer to the same physical memory address using VMA". However, the

section of Harvey to which the Examiner cites, column 2, lines 23-33, discloses processes of a main memory having virtual addresses for shared code and data. Harvey et al. does not disclose the element "the VMA referred to by each of the first and second instance of the program is the same" as recited in claim 1. Furthermore, Harvey et al. which discloses page tables in a main memory does not address the problem of and hence does not implicitly teach a VMA referred to by each of a first processor and a second processor as recited in claim 1.

For at least these reasons, claim 1 and its dependent claims are allowable over Harvey et al.

CLAIM 8

Claim 8 recites numerous limitations that are not taught or suggested in Harvey et al. By way of example, Claim 8 recites "referring to a virtual memory address (VMA) in a page table to locate the read/write variable, **wherein the VMA in each functional unit is the same**, and wherein the VMA in each functional unit contains a pointer to RAM within its functional unit". Moreover, Harvey et al. which discloses page tables in a main memory does not address the problem of and hence does not implicitly teach a VMA referred to by a plurality of functional units as recited in claim 8.

The applicants request that the Examiner particularly point out each and every element of the claimed invention to establish a *prima facie* case of obviousness or withdraw the rejection.

For at least these reasons, claim 8 and its dependent claims are allowable over Harvey et al.

CLAIM 12

Claim 12 recites numerous limitations that are not taught or suggested in Harvey et al. By way of example, Claim 12 recites "a page table in the first functional unit having a virtual memory address (VMA) for a read/write variable, the VMA in the page table of the first functional unit pointing to the first memory; and a second page table in the second functional unit having a VMA for the read/write variable, the VMA in the

page table of the second functional unit pointing to the second memory". Moreover, Harvey et al. which discloses page tables in a main memory does not address the problem of and hence does not implicitly teach a VMA referred to by each of a first functional unit and a second functional unit as recited in claim 12.

The applicants request that the Examiner particularly point out each and every element of the claimed invention to establish a *prima facie* case of obviousness or withdraw the rejection.

For at least these reasons, claim 12 and its dependent claims are allowable over Harvey et al.

CLAIM 16

Claim 16 recites numerous limitations that are not taught or suggested in Harvey et al. By way of example, claim 16 recites "a page table in the first functional unit having a virtual memory address (VMA) for a read/write variable, the VMA in the page table of the first functional unit pointing to the first means storing; and a second page table in the second functional unit having a VMA for the read/write variable, the VMA in the page table of the second functional unit pointing to the second means for storing".

Moreover, Harvey et al. which discloses page tables in a main memory does not address the problem of and hence does not implicitly teach a VMA referred to by each of the first and second means for executing programs being the same as recited in claim 16.

The applicants request that the Examiner particularly point out each and every element of the claimed invention to establish a *prima facie* case of obviousness or withdraw the rejection.

For at least these reasons, claim 16 and its dependent claims are allowable over Harvey et al.

III. Rejection of claims under 35 U.S.C. § 103

Claims 3-7 are rejected under 35 U.S.C. §103(a) as being unpatentable over Harvey et al. (U.S. Patent No. 6,233,668) as applied to claims 1 and 2, and further in view of de Backer et al. (U.S. Patent No. 6,266,745). The applicants respectfully traverse the rejections.

Claims 3-7 recite to independent claim 1 including a "performance counter". Admitting that Harvey et al. does not teach a performance counter, the Examiner alleges that de Backer et al. teachers a counter which keeps track of the shared memory accesses by each of a plurality of threads. Claims 3-7 recite numerous limitations that are not taught or suggested in either Harvey et al. or de Backer et al. By way of example, claim 3 recites a "performance" counter for writable data pointed to by a virtual memory address. Claim 4 recites combining the "count values" of a first and a second processor. Claim 5 recites the "performance counter count value" representing a number of page allocations in memory. Claim 6 recites a performance counter count value being a number representing a number of disk accesses. In contrast, de Backer et al. teaches using counter to determine the utilization of each of a plurality of nodes in a distributed shared-memory data processing system by each of a plurality of threads executed in the system. Backer et al. does not teach using performance counters with virtual memory. In fact de Backer et al. does not disclose any virtual memory system. Thus, de Backer et al. does not provide any motivation for combining its counters with the concurrent page tables of Harvey et al. to produce the system of claims 3-7.

The Examiner must provide *objective evidence*, rather than subjective belief and unknown authority, of the requisite motivation or suggestion to combine or modify the cited references. *In re Lee*, 61 U.S.P.Q.2d. 1430 (Fed. Cir. 2002). Obviousness cannot be established by combining the teachings of the prior art to produce the claimed invention absent some teaching or suggestion supporting the combination. *ACS Hospital Systems, Inc. v. Montefiore Hospital*, 732 F.2d 1572, 1577, 221 U.S.P.Q. 929, 933 (Fed. Cir. 1984). Such teaching or suggestion does not exist.

For at least these reasons, Applicant respectfully asks the Examiner to withdraw the rejection since a *prima facie* case of obvious has not been established.

IV. Conclusion

Claims 1-19 are believed to be in condition for allowance. Applicants respectfully requests reconsideration and prompt issuance of the present application. Should any issue remain that prevents immediate issuance of the application, the Examiner is encouraged to contact the undersigned attorney to discuss the unresolved issue.

Respectfully submitted,

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CERTIFICATE UNDER 37 C.F.R. 1.8

The undersigned hereby certifies that this paper or papers, as described herein, is being transmitted to the United States Patent and Trademark Office facsimile number 571-273-8300 on this 31st day of March 2006.

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